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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/448,884	11/24/1999	JOELLE SHARP	18865-003600	5563

20350 7590 09/09/2003

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EXAMINER
VU, DAVID

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/448,884	SHARP ET AL.	
	Examiner	Art Unit	
	DAVID VU	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) *15-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 19-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parekh et al.,(US 5,945,724) in view of Sato et al. (US 6,100,132).

Parekh et al, in related text (Col. 4, Line 18-Col. 6, Line 65) and figures (Figs. 1A-3) disclose a method of forming a trench in a semiconductor substrate, the trench defined by an open end at a major surface of the substrate and by a closed end within the body of the substrate, the method comprising the steps of: (a) providing a substrate10; (b) growing a masking layer 11/18 on the major surface of the substrate 10; c) selectively etching, through the masking layer 11/18 to the major surface of the substrate 10, to define a trench opening access; (d) anisotropically etching, from the trench opening access and into the body of the substrate 10 to form a trench; (Col. 4, Line 65-Col. 5, Line 12) (e) removing the selectively etched masking layer (Fig. 1G)

Parekh et al., disclose all claimed subject matter, but fails to expressly disclose annealing the trench in hydrogen ambient. Sato et al., in related text, (Col. 5, Lines. 40-46; Col. 6, Lines. 41-45; Col. 16, Lines. 37-40; Col. 19, Lines. 50-63; Col. 20, Lines. 45-62; Col. 21, Lines 3-6;) disclose the step of annealing the trench in hydrogen ambient with a temperature of between about 850-1200°C (Col. 19, Lines. 10-20) and pressure about 80Torr (Col. 14, Lines. 50-58) to reduce the number of defects in the trench created during the step of forming, and to round corners at the open and closed ends of the trench. However, given the substantial Parekh et al., in view of Sato et al., it would have been obvious to one with ordinary skill in the art at the time of the invention for annealing the trench to reduce the number of defects in the trench created during the step of forming, and to round corners at the open and closed ends of the trench. Since the trench shape in a silicon substrate can affect the electrical behavior of the trench, by shaping or rounding the corners of the trench to eliminate sharp corners, high electric fields are prevented, which in turn decreases the current leakage resulting from damaged trench sidewalls or implantation of materials along the sidewalls. The rounded shape of the trench with rounded bottom corners and rounded top corners also provides for ease in filling of the trench while reducing the critical dimension for the trench width. This allows a filler material of appropriate thickness to be used without formation of undesirable voids in the filled trench.

2. Claims 19-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu et al.,(US 5,943,581) in view of Sato et al. (US 6,100,132).

Lu et al., in related text, (Col. 4, Lines. 39-44; Col. 5, Lines. 37-41) and figures (Fig. 1-8) disclose a method of making a trench field effect transistor, comprising:

(a) providing a semiconductor substrate 10 of an N dopant charge type, the substrate embodying the drain of the trench field effect transistor (Col. 6, Lines. 19-32 and Fig. 8);

(b) growing an epitaxial layer 14 of the same N+ dopant charge type on the substrate 10, the epitaxial layer having a different resistivity than the resistivity of the substrate;

(c) growing a masking layer 22 on the major surface of the substrate 10 (Col. 6, Lines. 48-56);

(d) selectively etching, through the masking layer to the major surface of the substrate, to define a trench opening access; (Col. 6, Lines. 56-59)

(e) anisotropically etching, from the trench opening access and into the body of the substrate to form a trench; (Col. 7, Lines. 5-15)

(f) removing the selectively etched masking layer 22 (Col. 7, Lines. 28-30); and

(g) forming at least one trench into the epitaxial layer, each trench defined by a first end in a plane defined by a major surface of the substrate and by walls that extend to a second end at a predetermined depth into the epitaxial layer 14;

(h) growing a dielectric layer 26 on the walls of the at least one trench; (Col. 7, Lines. 30-44 and Fig. 7)

(i) forming a conductor 28 over the dielectric layer 26, the conductor embodying the gate of the trench field effect transistor; (Col. 7, Lines. 45-67 and Fig. 7)

(j) patterning the epitaxial layer and implanting a dopant of a second charge type to form p-wells interposed between adjacent trenches; (Fig. 7) and

(k) patterning the epitaxial layer and implanting a dopant of the n-type to form regions that embody the source regions of the field effect transistor. (Fig. 8)

Lu et al., disclose all claimed subject matter, but fails to expressly disclose the exposed sidewall surfaces of trench are annealed in a hydrogen ambient environment.

Sato et al., in related text, (Col. 5, Lines. 40-46; Col. 6, Lines. 41-45; Col. 16, Lines. 37-40; Col. 19, Lines. 50-63; Col. 20, Lines. 45-62; Col. 21, Lines 3-6;) disclose the step of annealing the trench in hydrogen ambient with a temperature of between about 850-1200°C (Col. 19, Lines. 10-20) and pressure about 80Torr (Col. 14, Lines. 50-58). However, given the substantial Lu et al., in view of Sato et al., it would have been obvious to one with ordinary skill in the art at the time of the invention for annealing the trench to reduce the number of defects in the trench created during the step of forming, and to round corners at the open and closed ends of the trench.

In re claim 20, Lu et al., in related text disclose further including the step of forming one or more heavy bodies of the second charge type positioned above the wells and between the source regions, each heavy body forming an abrupt junction with its corresponding well. (Col. 8, Lines. 33-67).

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is (703) 305-0391. The examiner can normally be reached on Monday-Friday from 8:00am to 5:00pm. If attempt to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms., can be reached on (703) 308-4910.

David Vu.
DV

David Nelms
Supervisory Patent Examiner
Technology Center 2800